ABSTRACT OF THE DISCLOSURE

The simulation apparatus of the present invention is a simulation apparatus that is intended for a pipeline processor that executes a plurality of instructions simultaneously, and it comprises a pipeline simulation unit operable to simulate a group of instructions comprising a plurality of instructions to be executed simultaneously and an instruction simulation unit operable to generate the simulation result of the group of instructions on an instruction-by-instruction basis based on the simulation result performed by the pipeline simulation unit, and the instruction simulation unit generates the simulation result by undoing the simulation where an instruction included in the group of instructions that has just been simulated by the pipeline simulation unit.